**Chandrakala Avula email:** [**chandu179544@gmail.com**](mailto:chandu179544@gmail.com) **Contact: 8498971392**

To obtain a challenging career in the field of DFT leading to professional as well as personal growth and to contribute to organization by utilizing my skills, knowledge and abilities.

# ACADEMIC QUALIFICATIONS

* **DFT** trained at CHIPEDGE Technologies Pvt Ltd, in January 2023.
* B. Tech (**ECE)** from Nalgonda Institute of Technology and Science, Nalgonda with an aggregate of **73.74%** in 2016.
* Intermediate (**MPC) f**rom Gouthami Junior College, Nalgonda with an aggregate of **83.4%** in 2012.
* **CBSE** from Aurobindo Public School, Nalgonda with an aggregate **of 8(CGPA)** in 2010.

# SKILLS & KNOWLEDGE

# Digital and Verilog concepts.

* Windows XP, LINUX.

**COURSE OUTLET**

* ASIC flow, DFT Fundamentals, SCAN Insertion, SCAN\_DRC, SCAN Compression, Boundary Scan, ATPG Pattern generation, Test coverage improvement, Simulation, BIST concepts**.**

**TOOLS USED IN TRAINING**

* **SYNOPSYS DFT Compiler** for SCAN, **Tetramax** for ATPG, VCSfor simulation**.**

**PROJECT-1 :** SCAN Insertion, ATPG on JBI DESIGN

* Technology : 28nm
* Design : Design with 8k cells
* NO. of Clocks : 3

### Tools Used : DFT compiler, TETRAMAX (tmax)

### Role : performed scan insertion by defining constraints and fixed DRC manually in

### scan mapped netlist, then generated patterns for stuck at and increased test

### coverage .

# PROJECT-2 : SCAN Insertion with compression, ATPG on JBI DESIGN

* Technology: 28nm
* Design : Design with 8k cells
* No.of Clocks : 3

### Tools Used : DFT compiler, TETRAMAX (tmax)

### Role : performed scan insertion by defining constraints, inserting compression logic DRC manually in scan mapped netlist, then generated patterns for stuck at and

increased test coverage.

**ACADEMIC PROJECTS**

1.Practical implementation of Rijndael S-BOX using combinational logic.

Combinational logic based Rijndael S-BOX implementation for the Sub Byte transformation in the Advanced Encryption Standard (AES) algorithm for Field Programmable Gate Arrays (FPGAs).

2.Wireless music transmission and reception with infrared.

### ACADEMIC ACHIEVEMENTS

* Participated in ANDROID APPLICATION DEVELOPMENT workshop in association with Virescent technologies pvt ltd.
* Presented a seminar on SNIFFER at national seminar on REAL TIME EMBEDDED SYSTEMS conducted at Mahatma Gandhi University, Nalgonda.

**STRENGTHS**

* Good communication skills
* Positive attitude
* Flexible
* Self-motivated

## PERSONAL INFORMATION

* Name : Chandrakala Avula.
* DOB : 17-06-1995.
* Languages known : English, Telugu, Hindi.
* Marital status : Married
* Address : 13-206/2, Medchal, Dist.
* Hobbies **:** Listening music, Reading books.

# DECLARATION

I **CHANDRAKALA AVULA**, here by declared that the information specified above is true to the best of my knowledge and understanding.